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EXAMINER	
HOGANS, DAVID L	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 04/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/926,377	GRASSL, THOMAS	
	Examiner	Art Unit	
	David L. Hogans	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Request for Continued Examination filed on February 23, 2004.

Status of Claims

Claims 11-18 are pending. Claims 1-10 are cancelled.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 11-18 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 11, 14-16 and 18 refer to "insulation elements". The Examiner interprets "insulation elements" to refer to layer 1 of Figure 1 (noting the scope of Claim 14). Applicant's specification at pages 2-3 denotes layer 1 as a silicon layer. Silicon is a semiconductor and not a insulator.

3. Claims 11-15 and 18 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 11 (lines 6-9) and 18 (lines 6-9) refer to a substrate "bearing vertically

integratable circuits". Figure 1 and Applicant's specification do not elucidate "vertically integratable circuits" existing before providing insulation elements with at least one gap.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 11-15 and 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Lines 12-13 of Claims 11 and 18 refer to "filling the at least one gap". This at least one gap is the gap formed during the step of field oxide formation (noting Claim 14 for clarification). These gaps then disappear due to field oxide formation. Therefore, no gaps exist that can be filled.

6. Claim 14 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Examiner is uncertain as to how the gaps are formed in the substrate in Claim 14 and the same gaps are formed within the insulation elements of Claim 11. According to Claim 11, insulation elements already exist before gap formation, and according to Claim 14, gap formation precedes insulation formation.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 16 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by 5,426,072 to Finnila.

In reference to Claim 16, Finnila teaches a vertically integratable circuit comprising:

- a substrate (12) bearing vertically integratable circuits (18 and 19b); (See Figures 2-10 and columns 3-8 lines 01-10)
- insulation elements (12 and 13) provided along a first side in a thickness direction of the substrate; (See Figures 2-10 and columns 3-8 lines 01-10)
- at least one gap (14a and 14b) formed within the insulation elements along the first side of the substrate; (See Figures 2-10 and columns 3-8 lines 01-10)
- active circuit elements (18) provided via the first side of the substrate; (See Figures 2-10 and columns 3-8 lines 01-10)
- at least one gap filled with an electroconductive material (16) extending from the first side of the substrate and forming at least one first side vertical contact; (See Figures 2-10 and columns 3-8 lines 01-10) and
- at least one second side vertical contact (28) formed of electroconductive material from the second side of the substrate extending therein at locations corresponding to the exposed at least one first side vertical contact (See Figures 2-10 and columns 3-8 lines 01-10)

Claim 17

In reference to Claim 17, Finnila teaches:

- wherein at least two vertically integratable circuits are connected, and electrically conductive contacts for vertical integration that are electrically connected with each other (See Figures 2-10 and columns 3-8 lines 01-10; noting Figure 8)

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over 5,426,072 to Finnila.

Claim 11

Finnila teaches a method for making a vertically integratable circuit consisting essentially the steps of: providing insulation elements (12 and 13) along a first side in a thickness direction of a substrate; forming at least one gap (14a and 14b) within the insulation elements along the first side of the substrate; providing the substrate with the active circuit elements (18) via the first side of the substrate; filling the at least one gap with an electroconductive material (16) from the first side to form at least one first side vertical contact; thinning the substrate (10) from a second side of the substrate opposite

the first side; etching at least one recess (contact openings) to expose at least one first side vertical contact; and applying electroconductive material (28) from the second side of the substrate at locations corresponding to the exposed at least one first side vertical contact (16) to form at least one second side vertical contact. (See Figures 2-10 and columns 3-8 lines 01-10)

Finnila fails to explicitly teach wherein the substrate bears vertically integratable circuits when providing insulation along a first side.

However, the specification contains no disclosure of either the critical nature of the claimed arrangement (providing insulation along a substrate bearing vertically integratable circuits) or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the claimed arrangements are critical. *In re Woodruff*, 919 F.2d 1575, 1578 (Fed. Cir. 1990)

In light of Applicant's failure to establish the criticality of forming the vertically integratable circuits before formation of the contacts for vertical integration, it is deemed equivalent to the formation of the contacts for vertical integration and then forming the vertically integratable circuits. The Examiner notes that Applicant's specification and drawings fail to teach wherein insulation is provided along a substrate already bearing vertically integratable circuits.

The Examiner notes that the phrase "consisting essentially the steps of" limits the scope of a claim to the specified material or steps "and those that do not materially affect the basic and novel characteristics" of the claimed invention. See MPEP § 2111.03 The Examiner contends the metallizations 21 and 23 do not materially affect the basic and novel characteristics because metallization 21 could be a bump electrode from another substrate and metallization 23 clearly need not be located over interconnect 16 according to the specification of Finnila.

Claim 12

Incorporating all arguments of Claim 11 and noting that Finnila teaches wherein the substrate has a hidden insulating layer and thinning is performed up to said insulating layer. (See Figures 2-10 and columns 3-8 lines 01-10)

Claim 13

Incorporating all arguments of Claim 11 and noting that Finnila, in columns 3-8 lines 01-10 and Figures 2-10, teaches a SOI substrate wherein thinning is performed up to the insulating layer.

The Examiner notes that Applicant's specification contains no disclosure of either the critical nature of the claimed process (i.e. – thinning until the insulation produced for the contacts for vertical integration is reached) or any unexpected results arising

therefrom. Where patentability is said to be based upon particular chosen processes or upon another variable recited in a claim, the Applicant must show that the chosen processes are critical. *In re Woodruff*, 919 F.2d 1575, 1578 (Fed. Cir. 1990).

Claim 18

Finnila teaches a method for making a vertically integratable circuit comprising the steps of: providing insulation elements (12 and 13) along a first side in a thickness direction of a substrate; forming at least one gap (14a and 14b) within the insulation elements along the first side of the substrate; providing the substrate with the active circuit elements (18) via the first side of the substrate; filling the at least one gap with an electroconductive material (16) from the first side to form at least one first side vertical contact; thinning the substrate (10) from a second side of the substrate opposite the first side; etching at least one recess (contact openings) to expose at least one first side vertical contact; and applying electroconductive material (28) from the second side of the substrate at locations corresponding to the exposed at least one first side vertical contact (16) to form at least one second side vertical contact. (See Figures 2-10 and columns 3-8 lines 01-10)

Finnila fails to explicitly teach wherein the substrate bears vertically integratable circuits when providing insulation along a first side.

However, the specification contains no disclosure of either the critical nature of the claimed arrangement (providing insulation along a substrate bearing vertically integratable circuits) or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the claimed arrangements are critical. *In re Woodruff*, 919 F.2d 1575, 1578 (Fed. Cir. 1990)

In light of Applicant's failure to establish the criticality of forming the vertically integratable circuits before formation of the contacts for vertical integration, it is deemed equivalent to the formation of the contacts for vertical integration and then forming the vertically integratable circuits. The Examiner notes that Applicant's specification and drawings fail to teach wherein insulation is provided along a substrate already bearing vertically integratable circuits.

1. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over 5,426,072 to Finnila in view of Silicon Processing for the VLSI Era (2000), volume 1, to Wolf et al.

Incorporating all arguments of Claim 11 and noting that Finnila teaches wherein insulation elements (13) are formed during production of field oxide but fails to explicitly teach wherein gaps formed in the substrate material enclose material that completely oxidizes during production of the field oxide.

However, Wolf et al., on pages 268-269, teaches the Deal and Grove model of silicon consumption versus the amount of final oxide thickness. Further, the Deal and Grove model teaches that a finitely thick quantity of silicon can be completely oxidized.

It would have been obvious to one of ordinary skill in the art to modify Finnila by incorporating substrate material that completely oxidizes during production of the field oxide, as taught by Wolf et al., to provide insulation and isolation regions for conducting elements.

2. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over 5,426,072 to Finnila in view of Semiconductor Manufacturing Technology (2001) to Quirk et al.

Incorporating all arguments of Claim 11 and noting that Finnila fails to explicitly teach wherein the gaps filled with electroconducive material are performed during production of a metallization level. The Examiner notes that Finnila does teach wherein routing metallization can be connected to vertical feedthroughs (16). See column 4 lines 49-58

However, Quirk et al., on page 301 teaches a copper metallization micrograph courtesy of Integrated Circuit Engineering wherein the vertical interconnects are filled

during production of a metallization level. Furthermore, Quirk et al. shows that metallization levels allow for a myriad of possible contacts between successive layers.

It would have been obvious to one of ordinary skill in the art to modify Finnila by incorporating vertical interconnects filled during production of a metallization level, as taught by Quirk et al., to allow for a myriad of possible contact points between successive layers.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 11, 16 and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by 6,104,081 to Dekker et al.

In reference to Claim 11, Dekker et al. teaches a method for making a vertically integratable circuit consisting essentially the steps of:

- providing insulation elements (3) along a first side in a thickness direction of a substrate; (See Figures 1-6 and columns 3-5 lines 20-53)
- forming at least one gap (19) within the insulation elements along the first side of the substrate; (See Figures 1-6 and columns 3-5 lines 20-53)
- providing the substrate with the active circuit elements (7-10) via the first side of the substrate; (See Figures 1-6 and columns 3-5 lines 20-53)
- filling the at least one gap with an electroconductive material (20) from the first side to form at least one first side vertical contact; (See Figures 1-6 and columns 3-5 lines 20-53)
- thinning the substrate (18) from a second side of the substrate opposite the first side and etching at least one recess to expose at least one first side vertical contact; (See Figures 1-6 and columns 3-5 lines 20-53) and
- applying electroconductive material (21) from the second side of the substrate at locations corresponding to the exposed at least one first side vertical contact (20) to form at least one second side vertical contact (See Figures 1-6 and columns 3-5 lines 20-53)

In reference to Claim 16, Dekker et al. teaches a vertically integratable circuit comprising:

- a substrate (1) bearing vertically integratable circuits (7-10); (See Figures 1-6 and columns 3-5 lines 20-53)

- insulation elements (3) provided along a first side in a thickness direction of the substrate; (See Figures 1-6 and columns 3-5 lines 20-53)
- at least one gap (19) formed within the insulation elements along the first side of the substrate; (See Figures 1-6 and columns 3-5 lines 20-53)
- active circuit elements (7-10) provided via the first side of the substrate; (See Figures 1-6 and columns 3-5 lines 20-53)
- at least one gap filled with an electroconductive material (20) extending from the first side of the substrate and forming at least one first side vertical contact; (See Figures 1-6 and columns 3-5 lines 20-53) and
- at least one second side vertical contact (21) formed of electroconductive material from the second side of the substrate extending therein at locations corresponding to the exposed at least one first side vertical contact (See Figures 1-6 and columns 3-5 lines 20-53)

In reference to Claim 18, Dekker et al. teaches a method for making a vertically integratable circuit comprising the steps of:

- providing insulation elements (3) along a first side in a thickness direction of a substrate; (See Figures 1-6 and columns 3-5 lines 20-53)
- forming at least one gap (19) within the insulation elements along the first side of the substrate; (See Figures 1-6 and columns 3-5 lines 20-53)
- providing the substrate with the active circuit elements (7-10) via the first side of the substrate; (See Figures 1-6 and columns 3-5 lines 20-53)

- filling the at least one gap with an electroconductive material (20) from the first side to form at least one first side vertical contact; (See Figures 1-6 and columns 3-5 lines 20-53)
- thinning the substrate (18) from a second side of the substrate opposite the first side and etching at least one recess to expose at least one first side vertical contact; (See Figures 1-6 and columns 3-5 lines 20-53) and
- applying electroconductive material (21) from the second side of the substrate at locations corresponding to the exposed at least one first side vertical contact (20) to form at least one second side vertical contact (See Figures 1-6 and columns 3-5 lines 20-53)

Response to Arguments

5. Applicant's arguments filed February 23, 2004, have been fully considered but they are not persuasive.

6. Initially, Applicant proffers, on page 8 second full paragraph, that "gaps" are formed after the circuitry is provided onto the substrate. When Claim 11 is read in context with Claim 14, the insulation elements are referring to layer 1 of Figure 1, which is a silicon layer that is later oxidized. Noting Figure 1a and 1b, the substrate bears no vertically integratable circuits. Therefore, no vertically integratable circuits exist when insulation elements are provided.

7. Next, Applicant argues that metallizations 21 and 23 of Finnila are the conductive contacts for vertical integration. The Examiner maintains that elements 16 are the vertical conductive contacts and that placing another metal layer over top of elements

16 does not change this property. Furthermore, the Examiner notes that metallization 21 could be a bump electrode from another substrate and metallization 23 clearly need not be located over interconnect 16 according to the specification of Finnila.

8. Next, Applicant portends that Claim 11 is a continuous process, thereby implying a sequential process. The Examiner notes there is no language within Claim 11 that provides a basis for a continuous or sequential step process.

9. Next, Applicant portends that indium bumps 23 are essential to Finnila's invention. The Examiner notes that Finnila clearly states that indium bumps 23 need not be located over vertical interconnect 16 and that indium bump 23 may also be a solder bump. The Examiner maintains that vertical interconnect 16 would be conductive regardless of the formation of indium bump 23, and therefore, indium bump 23 is incidental to the operation of Finnila.

10. Finally, the Applicant establishes criticality of forming vertically integratable circuits prior to the application of vertical contacts by stating:

> "Since finished substrates are no longer the starting point for introducing the vertical electric connections, an improved yield is obtained since no process steps which could change the already produced active circuit elements, such as steps with high process temperatures, are necessary any longer after production of the circuit elements."

This sentence states that finished substrates are no longer the starting point and then goes on to say that since circuit elements are already existing, no high thermal process steps are needed. This seems counterintuitive to Applicant's invention, because,

Applicant proffers that their invention begins with a finished substrate (i.e. - Applicant claims that vertically integratable circuits already exist). Conversely, if one reads Claim 11 and Claim 14 so as to provide parity between claimed subject matter, the substrate being employed in Figure's 1a and 1b are not finished because the active regions are yet to be formed. Clarification is needed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David L. Hogans whose telephone number is (571) 272-1691. The examiner can normally be reached on M-F (7:30-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

dh

Tuan H. Nguyen

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